**Arun Kumar E-mail**: arunav.kumar@gmail.com

**Mobile**: +91-9910097855

**Experienceoverview**

* 7.5years of experience in Wireless Physical Layer-1 development for LTE and GSM.
* Experience over various Uplink and Downlink components, source and channel coding, modulation, channel multiplexing, HARQ, MIMO, OFDM-A, HSDPA, HSUPA, Channel estimation, equalizers, error correction, L1-synchronization procedures, Doppler estimation, RSSI, SNR calculations.
* Expertise over expensive memory saving operations oriented firmware development, Data structure, DSP-Algorithm development, DSP-BIOS, DSP-peripheral programming e.g. AIF2, EDMA, EMIF, TIMERS, Multicore-IPC, MATLAB Simulink, C and Assembly and C++.

**Professional experience**: 7.5 Years

* *July 2012 – present(1 Year,3 months) Aricent Group, Gurgaon*
* *Dec-2010 - July 2012(1Year, 8 months) TATA Consultancy Services, Gurgaon*
* *July 2007 - Oct 2010(3 Years, 4 months) Robert Bosch India Pvt. Limited, Bangalore*
* *Feb 2006 - Apr 2007(1 Year, 3 months) Indian Telephone Industries, Bangalore*

**Technical leader at Aricent technologies, Gurgaon**

**Role &duties:** As a *Team Leader*, my responsibilities in Aricent are

* To understand the customer's reported problems/issues/bugs in DSP firmware and to propose the best solutionswithin specified time.
* To understanding and develop the DSP baseband functionalities and also make team members to understand about it.
* To participate in periodic technical meetings and knowledge share events.
* To timely report myimmediate supervisor about the task status updates and to discuss the fore coming risks in project.
* To participation in in-depth technical, code reviews and design specifications.

**Projects undertaken:**

* *(May-2013 – Present) Development of Multi-core DSP Baseband firmware, for the new BTS Hardware based on TMS320TCI6616 Quad-core Nyquist DSP processor.*

**Objective**: The objective of this project is to enhance the capacity of the existing Medusa NSN-BTS product from 6 carriers per DSP to 12 carriers per DSP. Old BTS was based on tri-core DSP without using the full feature of multicore communication, but this product will be using the full features of Multi-Core DSP.

**Responsibilities**: My responsibility is to analyze the feasibility and possible obstacles in firmware development. It comprises the detailed analysis of each functional library, new DSP BIOS development, IPC communication, crash debugging frame work and BTS functionality support analysis on new Hardware. Analysis of changes to be done in two types of different configuration of Composite cell multi-site architecture, changes to be done in Downlink and Uplink chain of baseband firmware.

**Role**: Development of fresh firmware for AIF2 interfaces. Inter DSP and Inter-core communication framework in DSP-multicore environment.

The objective of this project is to implementation the 4x4 MIMO model with HARQ (Hybrid Automatic Repeat request) as an improvement over the existing module of 2x2 MIMO. This improvement could compensate the multiple signal-to interference-and noise power ratios (SINRs) throughput of the as in conventional combining method to increase the overall throughput. The module base is IEEE 802.l6e Mobile WiMAX standards with LTE standards. Along with MIMO and HARQ, Intelligent Downlink Diversity over 4x4 antenna model will be the next phase of this project.

* *(Feb-2013 – May-2013) LTE: HARQ with MIMO, IDD (Intelligent Downlink Diversity), and DPP (Dynamic Power Pooling) featuresimplementation.*

**Objective**: The objective of this project is to implementation the 4x4 MIMO model with HARQ (Hybrid Automatic Repeat request)as an improvement over the existing module of 2x2 MIMO. This improvement could compensate the multiple signal-to interference-and noise power ratios (SINRs) throughput of the as in conventional combining method to increase the overall throughput. The module base is IEEE 802.l6e Mobile WiMAX standards with LTE standards. Along with MIMO and HARQ, Intelligent Downlink Diversity over 4x4 antenna model will be the next phase of this project.

* *(Dec-2012 – Apr-2013) High Speed Railway (HSR)with CMST feature (Composite Multi Site Transmission),3GPP feature development for Medusa NSN-BTS baseband firmware*

**Objective**: The objective of this functionality is to make or continue the calls over the speed 350Km/hour, especially for the countries having High Speed Railways. Doppler effects causes the link failure at speeds around 250-300 Km/h. At this speed the failure of decoding the TCH/Multi-framescauses the call drops.

**Responsibilities:**The prototyping of feature and implementation of the functionality is done in Clanguage. The newly implemented feature applies the Doppler correction in each DL packet; the Doppler value is extracted from each valid burst received in UL from main and diversity branch (combined) having SNR greater than 3dB, the average SNR of such 4 bursts is mapped according to the UL AFU table and the same is applied and sent to PCU (packet control unit), in Uplink U\_PS/CS frames. This U\_PS/CS frames are received in the DL and AFU bit field is extracted from UPS header and mapped according to the DL AFU table. This calculated value is applied as the Doppler correction in the Downlink frames. By doing so, the Doppler Effect is counter balanced and decoding of the packets/TCH frames is possible over the speed of 400Km/h.

* *(Sept-2012 – Dec-2012) ToP (Timing over Packet) Synch 3GPP feature development for Medusa, Epsilon and Odessa NSN-BTS basebandfirmware*

**Objective**: The objective of the functionality is to facilitate the BTS reset using the GPS clock rather than the master clock, without dropping the calls in affecting cells. This function will be effective when DFCA (Dynamic Frequency Channel Allocation) is enabled in the BTS topology. The BTS will operate in pseudo random hopping instead of cyclic hopping mode.

**Responsibilities:**To achieve the objective, I designed the functionality to provide the sync from the Global Positioning Clock arriving to the Location Manager Units (LMU), which was further connected to the BTS system. While DFCA is enabled on each of the TRX, the BTS operates in frequency hopping mode; the hopping frequencies are selected from theDMAL (Dynamic Mobile Allocation List) list. Whenever any of the BTS goes out of the Synch, the ToP Synch feature removes that BTS from the DFCA list and choose another BTS which is ready to switch from Master Clock to GPS clock, the removal is done to reduce the interference among the BB hoping frequencies. The new BTS switches its frequency hopping list from the MAL to DMAL list when ToP Synch is applied.

* *(Aug-2012 – Sept-2012)Receiver downlink quality sub (DLQualSub) for halfrate, full rate and enhanced full rate calls to reduce the receiver downlink degradation.*

**Objective**: The objective of this feature enhancement is to reduce the receiver downlink degradation by introducing the *DLQualSub* as a KPI parameter (Key Performance Indicator) while TFO (Tandem Free Operation) is ON and DTX (Discontinuous Transmission) is applied in downlink.

**Responsibilities:**To achieve the objective, I designed a functionality which can update the soft flag to check various SID frames in downlink when DTX is applied with TFO feature and DTX applied for HR, FR and EFR calls. Earlier, the *DLQualFul* was used to report this quality, and most of the mobile phones in field failed to decode the SID filler frames and reported the bad downlink quality and hence the bad downlink performance. This enhancement improved the reported DL quality by 3%.

**Hardware/software tools used:**CMW500, CMU300, AMU200, MAXI, SOFI, SMIQ, NSN-BTS Hardware (Epsilon, Medusa, Odessa), LMU, Wire-shark, M5 Abis logs analyzers, KPI analysis tools, Net-Hawk for Abis line configuration and generation, Clear-Case, Source Insight, NSN-EM for Site commissioning and configuration, MATLAB, Code Composer Studio 3.1, 3.3, 4.1, XDS-PP-Plus Emulator, VIM, different proprietary tools by Nokia Solutions Network, Perl TCL TK.

**IT analyst at TATA Consultancy Services, Gurgaon**

**Projects undertaken:**

* *(Sept-2011 – July-2012) UE conformance software modules for 3G Downlink power, UE Measurement report, Soft Handover (SHO), Hard Handover (HHO) for the client Rohde & Schwarz,Munich, Germany.*

**Objective**: The objective of this project is to design the RF test cases for the conformance testing of UE from different vendors. The test cases were designed using the MLAPI (Middle Layer API) framework provided by Rohde & Schwarz. The MLAPI framework is the typical state machine based approach to write the test cases and scripts. To write the TC we used the exposedfunctions in library which is usedto configure the Layer-1 and Layer-2 parameterswith the help of the GUI called *Contest*. I was appointed to understand and implement the test cases to achieve the testing of *3G Downlink power* in different fading conditions, to produce the *UE measurement reports* for different UE vendors like Nokia, Samsung, AT&T and Verizon, to design the software to simulate the *Soft Handover and Hard handover* scenarios using the Signal Simulator CMW500 and fading simulator AMU200.

* *(Dec-2010 – Aug-2011) Development of the 3GPP specs: TS45.005, TS45.119, 25.101 for Aeroflex, UK*

**Objective**: The objective of this project is to design and development of the various test cases for the conformance testing to the 3GPP test specs 45.005, 45.119, 25.101 for the client Nokia.

**Responsibilities:** Developed the RF test cases in C and C++. These test cases consists the development of test cases to test the*Error Vector Magnitude* (EVM) for 64-QAM modulation scheme, *Maximum output power, Minimum output power*, *Adjacent Channel Leakage Ratio (ACLR), Spectrum emission mask, Frequency error and Phase error, Reference sensitivity, Signaling reports IMEI, IMSI and power class, Inner and outer Loop Power Control, Occupied Bandwidth (OBW).*These TC were written in C and C++ to target the baseband simulator called Aeroflex 7100 and using the protocol stack called TM500.

**Hardware/software tools used:**TM500, Aeroflex-7100 Baseband simulator, Microsoft 2008 VC++, QXDM logs analyzer, test UE’s from Qualcomm, Nokia and Samsung, MATLAB for crash dump analysis.

**Software Engineer at Robert Bosch India Pvt. Limited, Bangalore**

In Bosch, I participated in implementation and development of various DSPalgorithms, embedded software enhancement, bug fixing, feature development, module and system testing, software profiling, critical analysis, result validation and verification. The major work was to deal with the real time data obtained from various sensors and actuators positioned at the specific locations in engine and vehicle body. This data carries the information about the temperature, pressure, humidity, and air-fuel ratio, NOX presence in exhaust, EGR and Induction volume in Engine manifolds. During work, I obtained expertise on auto-code generation via ASCET and MATLAB tools. I also involved in developed of variousAUTOSAR libraries in MATLAB and Simulink for PSA.

I extensively worked on ETAS which provides measurement, calibration, and diagnostic development facility to automakers and suppliers worldwide. I worked on INCA and ETAS ECU and bus interfaces along with measurement modules to calibrate, validate, and diagnose automotive electronic systems and ECU which acquires the reliable data from those systems and the vehicle environment. I worked for customers like Hyundai, Nissan, Porsche, BMW and PSA.

* *Injection modeling using KALMAN filter*

**Responsibilities:**As a part of team of 5 people, we developed the sensor-less control system using 2nd order modified KALMAN filter in Boost control components for the client Porsche. The filter was designed on the pattern of a motor model used in the field oriented control system. The KALMAN filter’s job was to decide the modeled value or the Sensor value at a particular moment of time during injections in cylinders. It helped in altitude correction based fuel injectors and to supply power to engine during the hilly drive. This project was specifically designed for the customer Porsche, for twin flow engines. After successful implementation, the project was adopted by Hyundai motors and B.M.W also. The software was written in C++ and C.

**Hardware/software tools used:**INCA, ETAS ECU, CAN Tools as CANoe, CANape, TAE, MS-IDE 2008, ASCET, MATLAB, Code Composer Studio, SDOM and Clear Case, BA Converter, Active-Perl 5.10

**Engineer R&D at Indian Telephone Industries Ltd, Bangalore**

I was recruited in Digital Signal Processing R&D department for the project *Smart Exchange* for Indian Air force. The Smart Exchange has three main components Master Card, Slave Card, Operator Console unit, and different types of wire-lined subscribers connected to PSTN e.g. Magneto, Make-Brake, DTMF, trunk.

*Master card* is the main call processing unit controlled by a fixed point TI-DSP processor TMS320C6211. The master card is fabricated in 6 highly dense layered PCB board with DSP processor and its peripheral chips on-board, and other supporting embedded SoC e.g. EPROM, SDRAM, McBSP ports, Vertex 5 FPGA, Multi-tone chips, Conference Chip, Level Convertor IC's, Digital Switches and PC Bridge slots to connect with the PC mother board. I am the part of the DSP processor programming and hardware design team.

*Slave Card* having the amplifiers and line connection jacks to support Magneto, DTMF, dual VoIP speech codec TLV320AIC23, which connects the wired lines to the interface ports available on slave card. This card was designed by the line control department.

*Operator console unit* designed for the person sitting at the operator’s desk, the operator can hold maximum up to 6 subscribers routed by the master card. This card already existedwith ITI.

**Responsibilities:**I participated in writing the TI-DSP firmware for the Master Card DSP processor, Vertex-5 FPGA and various supporting chips. I implemented the Goertzel's algorithm under the guidance of Texas Instruments development center and DGMR-SP (DSP-Group) for DTMF detection and bits validation. Also, written the code for Conference chips to support 32 subscribers, WIN API for PC Bridge and UART at McBSP ports. The firmware was the size of around 50KLOC. I also designed a flash burn utility in Visual C++ that flashes the Hex file on on-board DSP memory chip. It was successfully programmed the glue-less Mitel FLASH memories through 14 pin-JTAG port. During this project I achieved many recognitions and successes and got expertise in logical memories interfacing and FLASH with DSP processors.

**Hardware/software tools used:**Microsoft IDE Visual basic 2008 for C++ code development, C, BIOS and MATLAB, Code Composer Studio for TMS320C64xx DSP Processor, SDOM and Clear Case.

**Paper presentations/publications**

* Presented white paper on feasibility of reduced handovers with the architecture of Composite Multi-site in GSM environment. – December,-2012, NSN-Aricent Techfest.
* *New model of time & feasibility of time machine*, IT-BHU, 4th Prastuti IEE Conference-2005
* *Proposed architecture of Digital Signal Processors*, IIT-Delhi, Paper-2005
* *Nanotechnology*, NIT-SHSL-CIET, Longowal National-Technical Festival-2004
* *Multiple Access System: WCDMA*,Second prize, ISTE-Lucknow-2005

**Certifications and trainings**

* May-2009: “*Device Drivers, Linux interns and VxWorks hands-on training*” at Kiona Software institute- Bangalore.
* Jan-2009: “*A1 certification in proficiency of German language*” Goethe Institute, Max-Mueller Bhavan, Bangalore, sponsored by Bosch
* May-2008: “*Automotive control system project and training on MATLAB and Simulink*” at Bosch, by Dr. S.R. Shankapal, M.S.Ramaiah School of Advanced Studies, Bangalore.
* May-2004: 3 *Internship in CDMA2000, GSM, WCDMA and Wireless in Local Loop (WLL) technologies,* ALTTC-Ghaziabad, India
* May-2003: *Internship in QA-C, fabrication of ceramic & photovoltaic cells in Fab lab at Central Electronics Ltd, Sahibabad, India.*

**Education qualification**

* B. Tech (2001-2005), Electronics & Communications, KIET-Ghaziabad, 73%.
* 12th (1998), S.D. Inter College, Ghaziabad, U.P Board of Education, 68%.
* 10th (1996), S.D. Inter College, Ghaziabad, U.P Board of Education, 72.3%.

**Academic projects**

* *IEEE Project: Utility Interactive Inverter System for Small Distributed Generation, by*“International Future Energy Challenge™”, Student Competition-2005.
* *Web link*: ***http://www.energychallenge.org/mainIFEC2005.htm***
* *Sponsors*: IEEE, Power Electronics Society, IEEE-IES, IEEE-IAS, SUKAM Inverters.

***Mentors:***

* Dr. Sanjay Gairola, PhD, IIT Delhi.
* Mr. Ajai Singh, M.Tech, IIT Kharagpur.
* Mr. Ravi Gupta, M.Tech IIT-Delhi.

**Objective**: The objective of the project is to construct a single phase inverter system. The inverter should be single phase operated from DC input voltage of range 30-60V, with 90% energy efficient. The input power variation should be limit to 250W to 1000W, to a single-phase utility line 110/240V at 50/60Hz. The project has to be designed under 115 design constraints proposed by IEEE. These constraints include the number of electronics components on mother board, form factor, power factor, and efficiency at each stage of design etc.

I was responsible to the design the simulation model of the PWM generation concept in MATLAB Simulink. This PWM code was finally optimized for TMS320C2407LF DSP. I was involved in design, prototyping and writing C and Assembly code for the DSP generation of theBuck-Boost converter module.

* *Micro-controller 89C51 based Elevation Control System. Jan-2005 to Mar-2005*

**Objective**: This objective of this project was to control a DC Unipolar motor and made it to work like an elevator system. Motor’s up, down and stop behavior was precisely designed and calibrated with 8051 microcontroller. The micro-controller was designed to produce 6 variable motions in up and down direction. I introduced several attractive features in this project like pass floors on priority and overweight detection and very slow motion in choosing specific options.

**Other details**

* Date of birth: 02-December-1980
* Passport: E9059737 (valid till 2014)
* Language: Hindi, English, German (A1)